Features

- **Supply Voltage: 5 V**
- **Low Power Consumption: 15 mA/5 V**
- **Output Level and Spurious Products Adjustable (Optional)**
- **Excellent Sideband Suppression by Means of Duty Cycle Regeneration of the LO Input Signal**
- **Phase-control Loop for Precise 90° Phase Shifting**
- **Power-down Mode**
- **Low LO Input Level: -15 dBm**
- **50-Ω Single-ended LO and RF Port**
- **LO Frequency Range of 30 MHz to 300 MHz**

Lead Free

Benefits

- **Low Current Consumption**
- **Few External Components Result in Cost and Board Space Saving**
- **Adjustment Free Hence Saves Time**

Electrostatic sensitive device.
Observe precautions for handling.

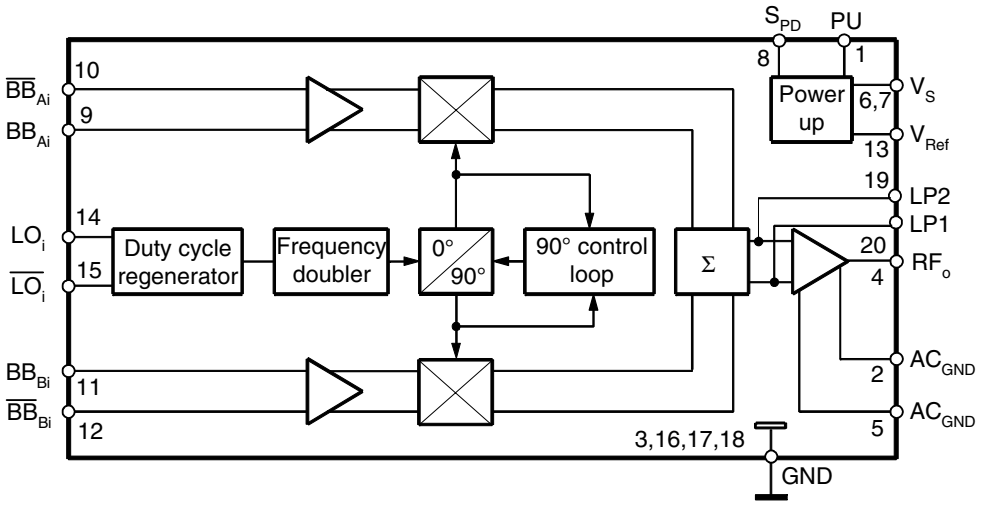
300-MHz Quadrature Modulator

U2793B

Description

The IC U2793B is a 300-MHz quadrature modulator that uses Atmel's advanced UHF process. It features low current consumption, single-ended RF ports and adjustment-free application, which makes the device suitable for all digital radio systems, e.g., GSM, PCN, JDC and WLAN. As an option, output level and spurious products are adjustable at pins 19 and 20. In conjunction with Atmel's U2795B mixer, an up-converter up to 2 GHz can be realized.

Figure 0-1. Block Diagram



Rev. 4651D–CELL–03/05

1. Pin Configuration

Figure 1-1. Pinning SSO20

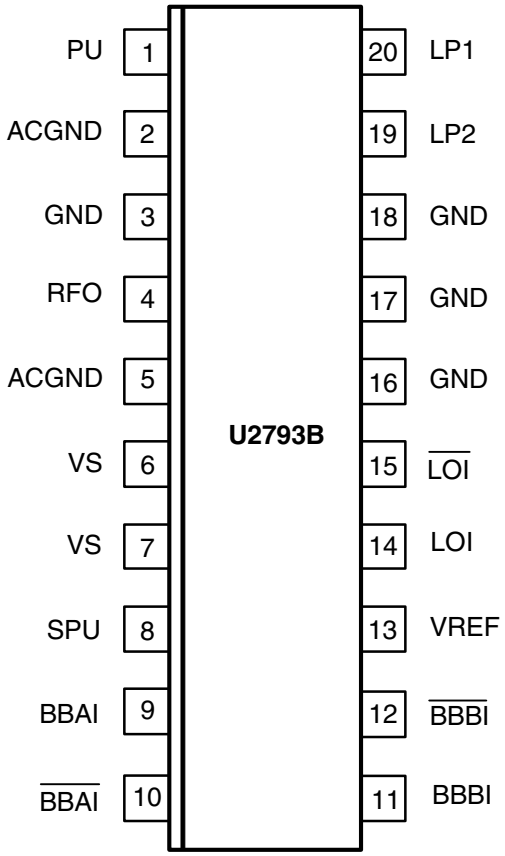


Table 1-1. Pin Description

Pin	Symbol	Function
1	PU	Power-up input
2	ACGND	AC ground
3	GND	Ground
4	RFO	RF output
5	ACGND	AC ground
6	VS	Supply voltage
7	VS	Supply voltage
8	SPU	Settling time power-up
9	BBAI	Baseband input A
10	BBAI	Baseband input A inverse
11	BBBI	Baseband input B
12	BBBI	Baseband input B inverse
13	VREF	Reference voltage (2.5 V)
14	LOI	Input LO
15	LOI	Input LO inverse, typically grounded
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	LP2	Output low pass and power control
20	LP1	Output low pass and power control

2. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage	V_S	6	V
Input voltage	V_i	0 to V_S	V
Junction temperature	T_j	125	°C
Storage temperature range	T_{Stg}	-40 to +125	°C

3. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO20	R_{thJA}	140	K/W

4. Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	V_S	4.5 to 5.5	V
Ambient temperature range	T_{amb}	-40 to +85	°C

5. Electrical Characteristics

Test conditions (unless otherwise specified); V_S = 5 V, T_{amb} = 25°C, referred to test circuit.
System impedance Zo = 50 Ω, f_{LO} =150 MHz, P_{LO} = -15 dBm, V_{BBi} = 1.0 V_{pp}, differential

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	Supply voltage range		6, 7	V_S	4.5	5	5.5	V	A
1.2	Supply current		6, 7	I_S		15		mA	A
2	**Baseband Inputs, Pin 9-10, 11-12**								
2.1	Input-voltage range (differential)			V_{BBi}		1000	1500	mVpp	D
2.2	Input impedance			Z_{BBi}		30		kΩ	D
2.3	Input-frequency range			f_{BBi}	0		50	MHz	D
2.4	Input voltage, common mode					2.5		V	
3	**LO Input, Pins 14 and 15**								
3.1	Frequency range			f_{LOi}	30		300	MHz	D
3.2	Input level[1]			P_{LOi}		-15	-5	dBm	D
3.3	Input impedance			Z_{iLO}		(2)		Ω	D
3.4	Voltage standing wave ratio			$VSWR_{LO}$		3.5			D
3.5	Duty-cycle range			DCR_{LO}	0.4		0.6		D

Notes:
1. Required LO level is a function of the LO frequency.
2. The LO input impedance is consisting of a 50 Ω resistor in series with a 15 pF capacitor.
3. With the pins 19 and 20 spurious performance especially for low frequency application can be improved by adding a chip capacitor between LP1 and LP2. In conjunction with a parallel resistor the output level can be adjusted to the following mixer stage without degration of LO suppression and noise performance which would decrease if the I/Q input level is reduced.
4. For T_{amb} = -40°C to +85°C and V_S = 4.5 V to 5.5 V

5. Electrical Characteristics (Continued)

Test conditions (unless otherwise specified); V_S = 5 V, T_{amb} = 25°C, referred to test circuit.
System impedance Zo = 50 Ω, f_{LO} =150 MHz, P_{LO} = -15 dBm, V_{BBi} = 1.0 V_{pp}, differential (Continued)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4	**RF Output, Pin 4**								
4.1	Output level	f_{LO} = 150 MHz, V_{BBi} = 1 V_{pp}, differential f_{LO} = 50 MHz, V_{BBi} = 0.3 V_{pp}, differential		P_{RFo}	- 3	-1 0	+2	dBm	A/B
4.2	LO suppression	P_{LO} = -20 dBM		LO_{RFO}	32	45		dB	A
4.3	Voltage standing wave ratio			$VSWR_{RF}$		1.4	2		D
4.4	Sideband suppression(3)			SBS_{RFo}	35	45		dB	A
4.5	Phase error(4)			Pe		< 1		deg	D
4.6	Amplitude error			Ae		< ±0.25		dB	D
4.7	Noise floor	V_{BBi} = 2 V, V_{BBi} = 3 V V_{BBi} = V_{BBi} = 2.5 V		N_{FL}		-137 -143		dBm/Hz	D
5	**Power-up Mode**								
5.1	Supply current	V_{PU} ≤0.5 V, pins 6, 7 V_{PU} = 1 V		I_{PU}		10	1	µA	D
5.2	Settling time	Pins 1 to 4, C_{SPU} = 100 pF C_{LO} = 100 pF, C_{RFo} = 1 nF		t_{SPU}		10		µs	D
6	**Switching Voltage, Pin 1**								
6.1	Power on			V_{PUON}	4			V	D
7	**Reference Voltage, Pin 13**								
7.1	Voltage range			V_{Ref}	2.375	2.5	2.625	V	A
7.2	Output impedance			Zo_{Ref}		30		Ω	D

Notes:
1. Required LO level is a function of the LO frequency.
2. The LO input impedance is consisting of a 50 Ω resistor in series with a 15 pF capacitor.
3. With the pins 19 and 20 spurious performance especially for low frequency application can be improved by adding a chip capacitor between LP1 and LP2. In conjunction with a parallel resistor the output level can be adjusted to the following mixer stage without degration of LO suppression and noise performance which would decrease if the I/Q input level is reduced.
4. For T_{amb} = -40°C to +85°C and V_S = 4.5 V to 5.5 V

6. Diagrams

Figure 6-1. Reference Voltage versus T_{amb}

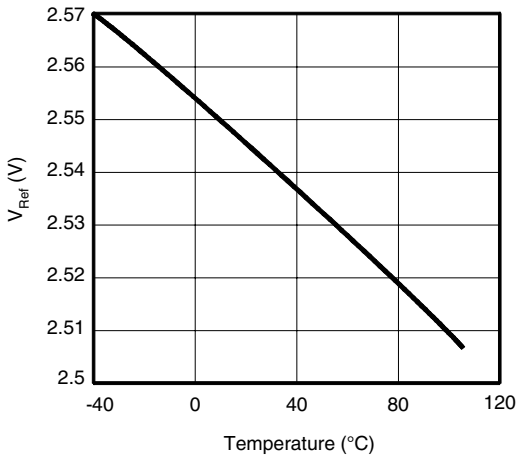


Figure 6-2. OIP3 versus T_{amb}, LO = 150 MHz, Level -10 dBm

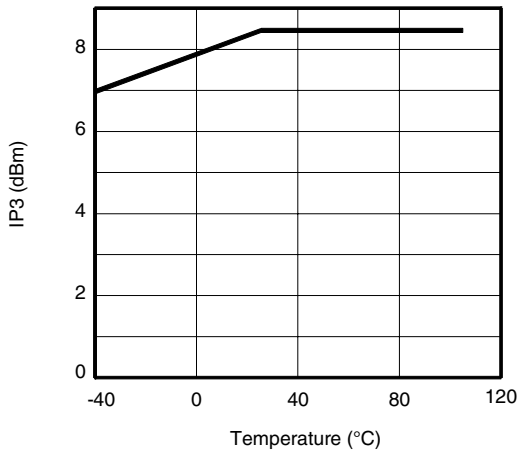


Figure 6-3. Supply Current versus T_{amb}

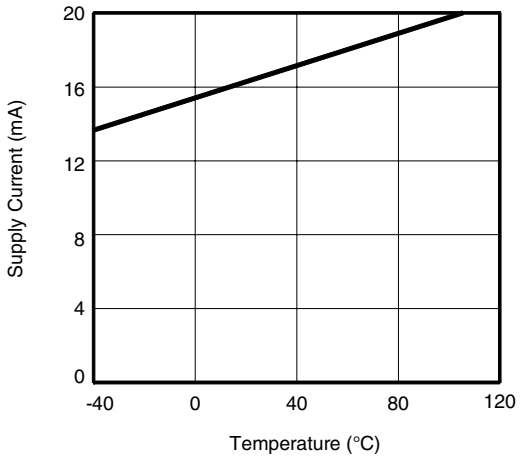


Figure 6-4. Recommended LO Power Range versus LO Frequency at T_{amb} = 25° C

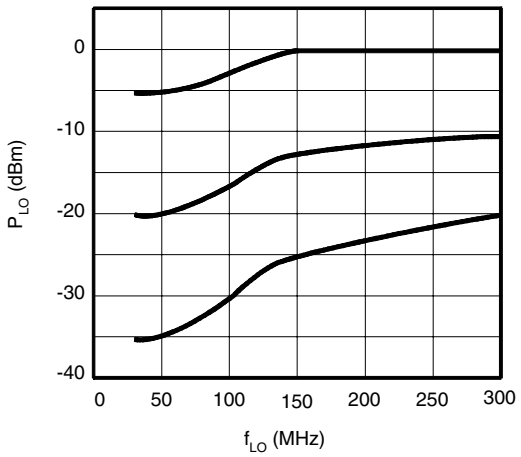


Figure 6-5. Output Power versus T_{amb}

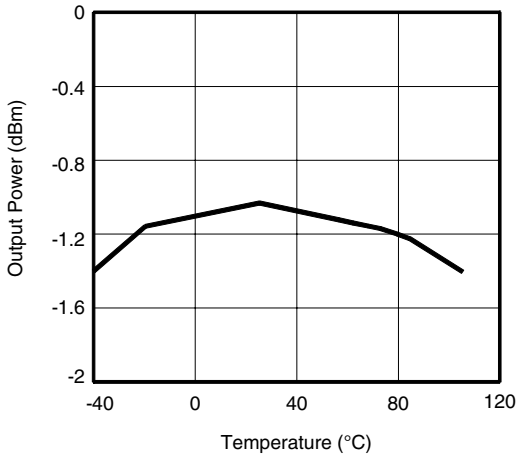


Figure 6-6. Typical Output Power versus LO Frequency at T_{amb} = 25° C, V_{BBi} = 250 mV (Differential)

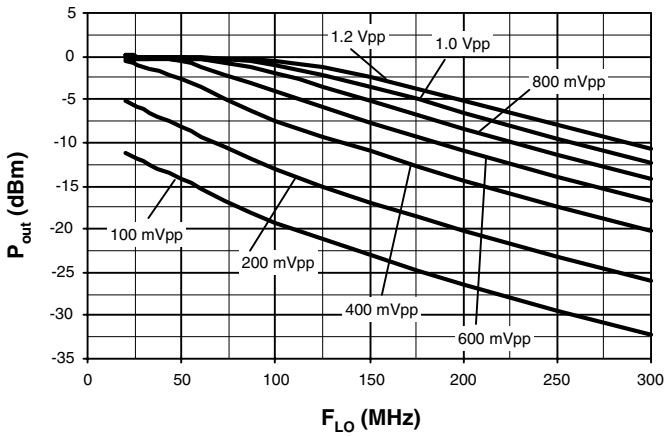
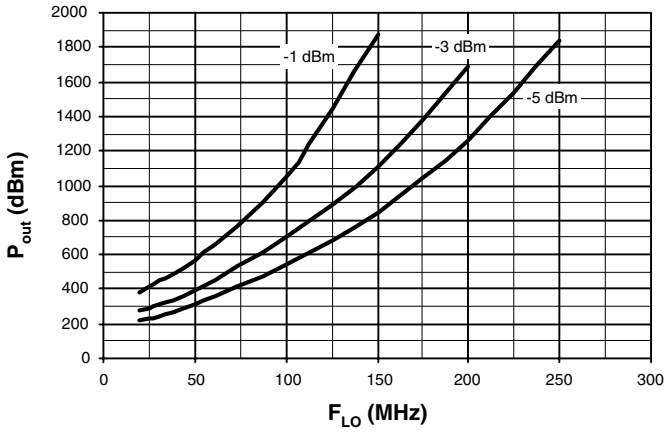
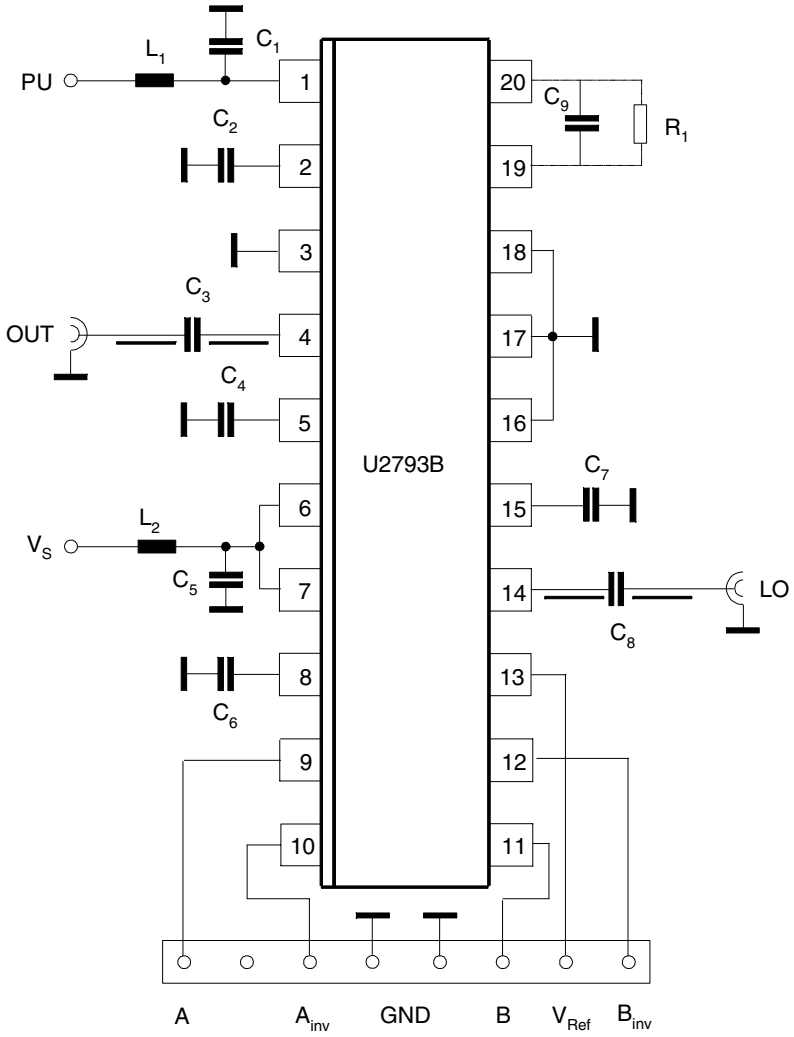


Figure 6-7. Typical Required V_{BBi} Input Signal (Differential) versus LO Frequency for P_O = 1 dBm and P_O = -3 dBm



7. Evaluation Board Drawings

Figure 7-1. Evaluation Board Circuitry

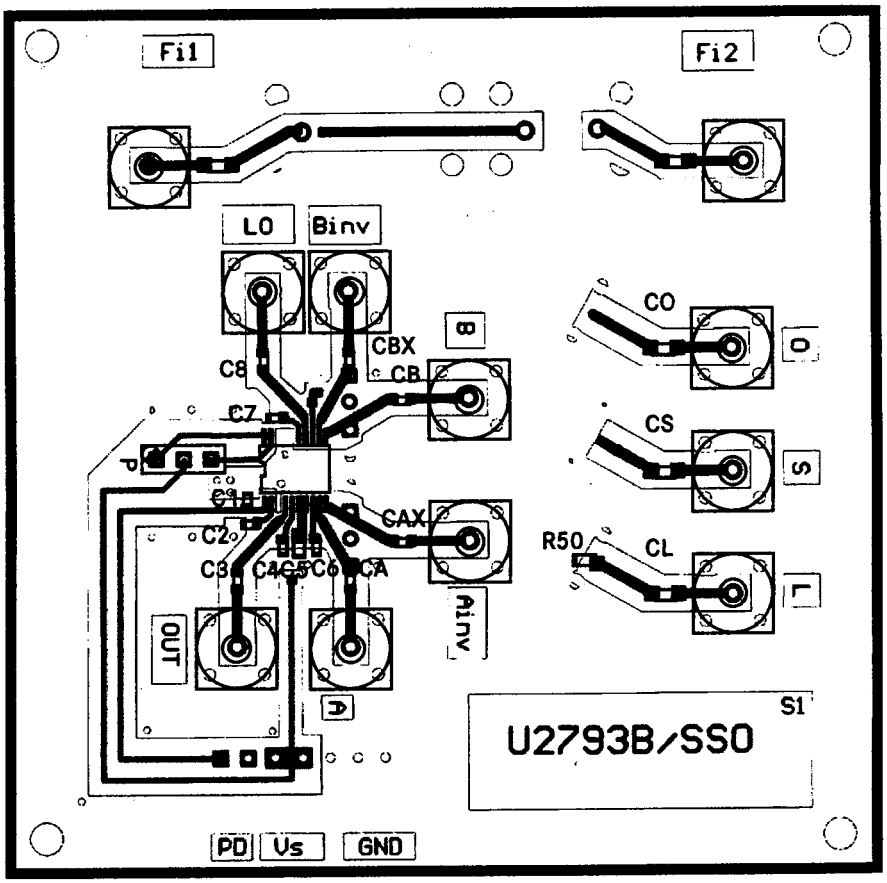


Part List

C_1, C_2, C_3, C_4, C_6	=	1 nF
C_7, C_8	=	100 pF
C_5	=	100 nF
C_9, R_1	=	1 pF to 10 pF
═══	=	50-Ω Microstrip
_ — — _	=	optional

The above listed components result in a PD settling time of <20 µs. The use of other component values will require consideration for time requirements in burst-mode applications.

Figure 7-2. PCB Layout Evaluation Board



8. Application Circuits

Bias network for AC-coupled baseband inputs (V_{BA}, V_{BB}).

R_1 = 2.5 kΩ, R_2 ≤10 kΩ for ≥ 35 dB LO suppression which is in reference to < 2 mV input offset.

Figure 8-1. Application Circuit with AC-coupled Baseband Inputs

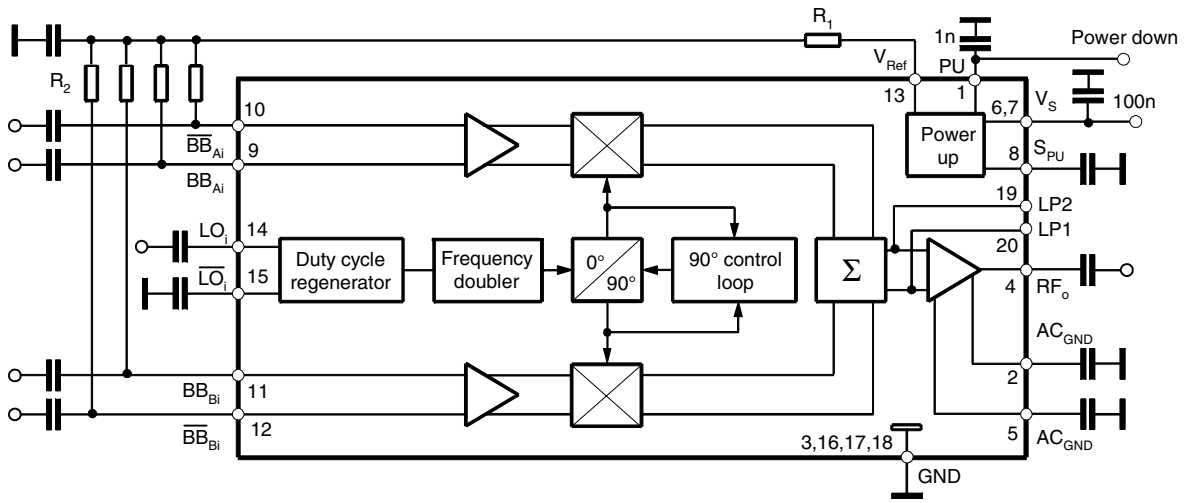
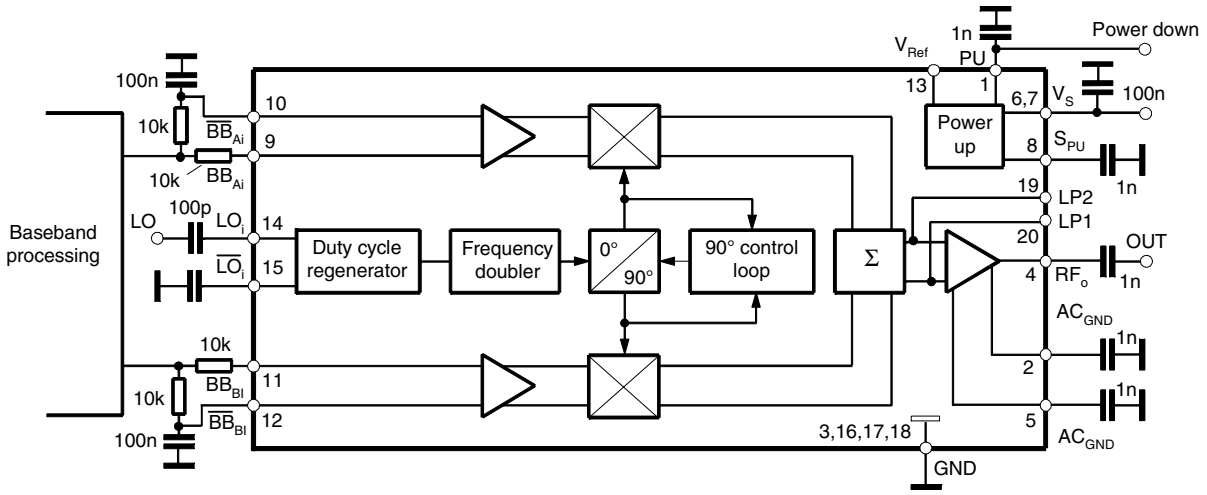


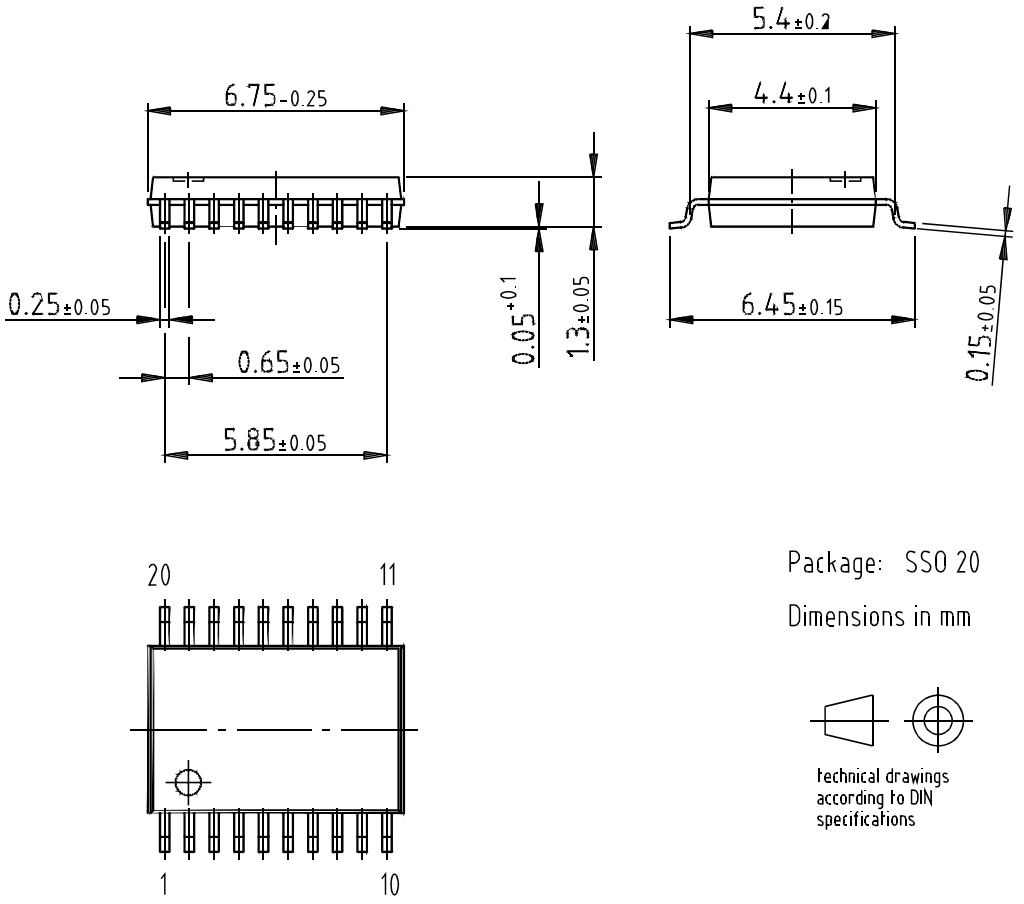
Figure 8-2. Application Circuit with DC-coupled Baseband Inputs



9. Ordering Information

Extended Type Number	Package	Remarks
U2793B-NFSH	SSO20	Tube, lead free
U2793B-NFSG3H	SSO20	Taped and reeled, lead free

10. Package Information



Drawing-No.: 6.543-5056.01-4
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